

What is claimed is:

1 1. A stacked gate vertical flash memory, comprising:
2 a semiconductor substrate with a trench;
3 a source conducting layer, formed on a bottom of the
4 trench;
5 an insulating layer, formed on the source conducting
6 layer;
7 a gate dielectric layer, formed on a sidewall of the
8 trench;
9 a conducting spacer, formed on the gate dielectric layer
10 as a floating gate;
11 an inter-gate dielectric layer, covered on the
12 conducting spacer; and
13 a conducting control gate filled in the trench.

1 2. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the source conducting layer comprises a
3 polysilicon layer or an epi-silicon layer

1 3. The stacked gate vertical flash memory as claimed in
2 claim 2, wherein the source conducting layer is a doped As
3 ion layer.

1 4. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the source conducting layer can be a common
3 source.

1 5. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the insulating layer comprises an oxide
3 layer.

1 6. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the gate dielectric layer comprises a gate
3 oxide layer.

1 7. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the top portion of the conducting spacer is
3 a tip.

1 8. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the conducting spacer comprises a polysilicon
3 layer or an epi-silicon layer.

1 9. The stacked gate vertical flash memory as claimed in
2 claim 1, wherein the inter-gate dielectric layer comprises
3 a gate oxide layer.

1 10. The stacked gate vertical flash memory as claimed
2 in claim 1, wherein the second conducting layer comprises a
3 polysilicon layer or an epi-silicon layer.

1 11. The stacked gate vertical flash memory as claimed
2 in claim 1, further comprises a source area formed on a side
3 of the insulating layer in the semiconductor substrate,
4 wherein the source comprises an As ion implanted area.

1 12. The stacked gate vertical flash memory as claimed
2 in claim 1, further comprises a drain area formed on a side
3 of the top of the conducting spacer in the semiconductor
4 substrate, wherein the drain comprises an As ion implanted
5 area.

1 13. The stacked gate vertical flash memory as claimed
2 in claim 1 further comprises an isolation oxide layer for

3 separating the source conducting layer and the semiconductor
4 substrate.

1 14. A stacked gate vertical flash memory, comprising:
2 a semiconductor substrate with a trench, wherein an
3 isolation layer is formed on a bottom of the trench;
4 a source conducting layer, formed on the bottom of the
5 trench, wherein the source conducting layer and the
6 semiconductor substrate are separated by the
7 isolation layer;
8 an insulating layer, formed on the source conducting
9 layer, wherein the insulating layer and others
10 formed thereon are separated by the insulating
11 layer;
12 a gate dielectric layer, formed on a sidewall of the
13 trench;
14 a conducting spacer, formed on the gate dielectric layer
15 as a floating gate;
16 a source area, formed on a side of the insulating layer
17 in the semiconductor substrate, wherein the
18 conducting spacer electrically connected to the
19 source conducting layer and the conducting spacer;
20 a drain area, formed on a side of a top of the conducting
21 spacer;
22 an inter-gate dielectric layer, covered on the
23 conducting spacer; and
24 a control gate conducting filled in the trench.

1 15. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the source conducting layer comprises
3 a polysilicon layer or an epi-silicon layer

1 16. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the source conducting layer is an As ion
3 doped layer.

1 17. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the insulating layer comprises an oxide
3 layer.

1 18. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the gate dielectric layer comprises a
3 gate oxide layer.

1 19. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the top portion of the conducting spacer
3 is a tip.

1 20. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the conducting spacer comprises a
3 polysilicon layer or an epi-silicon layer.

1 21. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the source conducting layer can be an
3 As ion doped layer.

1 22. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the drain conducting layer can be an As
3 ion doped layer.

1 23. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the inter-gate dielectric layer comprises
3 a gate oxide layer.

1 24. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the control gate conducting layer
3 comprises a polysilicon layer or an epi-silicon layer.

1 25. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the isolation layer comprises an oxide
3 layer.

1 26. A method for fabricating a stacked gate vertical
2 flash memory, comprising:

3 providing a semiconductor substrate, wherein a trench
4 is formed in the semiconductor substrate;
5 conformally forming an isolation layer on a bottom of
6 the trench;

7 forming a source conducting layer on the bottom of the
8 trench, wherein the source conducting layer and the
9 semiconductor substrate are separated by the
10 isolation layer;

11 conformally forming an ion doped insulating layer on a
12 sidewall of the trench and the source conducting
13 layer;

14 annealing the ion doped insulating layer, wherein the
15 dopant is driven in to the semiconductor substrate
16 of the bottom of the trench to form a source area,
17 the dopant is driven in the source conducting layer
18 to form a common source area, and the source area
19 and the common source area are connected;

20 removing the doped ion insulating layer;

21 forming an insulating layer on the source conducting
22 layer, wherein the source conducting layer and

23 others formed thereon are separated by the
24 insulating layer;
25 sequentially forming a gate dielectric layer and a
26 conducting spacer on the sidewall of the trench,
27 wherein the conducting layer covers the gate
28 dielectric layer as a floating gate, and a top
29 portion of the conducting spacer is a tip;
30 dopant implanting into the top of the conducting spacer
31 to form a drain area on a side of the top of the
32 conducting spacer in the semiconductor substrate;
33 forming an inter-gate dielectric layer covering the
34 conducting layer; and
35 filling a control gate layer in the trench.

1 27. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the source conducting layer comprises
3 a polysilicon layer or an epi-silicon layer

1 28. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the insulating layer comprises an oxide
3 layer.

1 29. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the gate dielectric layer comprises a
3 gate oxide layer.

1 30. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the conducting spacer comprises a
3 polysilicon layer or an epi-silicon layer.

1 31. The stacked gate vertical flash memory as claimed
2 in claim 14, wherein the dopant comprises As ions.

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1 32. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the inter-gate dielectric layer comprises
3 a gate oxide layer.

1 33. The stacked gate vertical flash memory as claimed
2 in claim 26, wherein the control gate conducting layer
3 comprises a polysilicon layer or an epi-silicon layer.